## ABSTRACT OF THE DISCLOSURE

A data transmission circuit includes a control signal generation circuit, a write state machine, a conversion circuit, a read state machine, and a selection circuit. The control signal generation circuit receives a strobe signal and a clock signal in response to an enable signal, generates a write control signal that is activated in response to a rising edge of the strobe signal, and generates a read control signal that is activated in response to a first rising or falling edge of the clock signal after the write control signal is activated. The write state machine is activated in response to the write control signal, changes its internal state in synchronization with the strobe signal, and sequentially outputs input control signals in response to the changed internal state. The conversion circuit converts serial data to parallel data in response to the input control signal sequentially output from the write state machine and latches the parallel data. The read state machine is activated in response to the read control signal, changes its internal state in synchronization with the clock signal, and sequentially outputs output control signals in response to the changed internal state. The selection circuit outputs the parallel data latched in the conversion circuit in the same order that the serial data is sequentially input to the conversion circuit in response to the output control signals sequentially output from the read state machine.